WE CLAIM:

1. A DC-DC converter which produces a regulated output voltage and which uses the instantaneous output voltage to establish the duty ratio required for maintaining said output voltage, comprising:

at least one switching element connected between an input voltage and a first node;

an output inductor connected between said first node and an output terminal; and

a switching control circuit which cycles said switching element on and off to maintain a desired output voltage at said output terminal, each of said switching cycles comprising an "on" time interval T_{on} during which said switching element is on and connects said first node to said input voltage, and an "off" time interval T_{off} during which said switching element is off and disconnects said first node from said input voltage, said switching control circuit comprising:

a resistive network connected to produce a feedback voltage V_{fb} at a feedback node representative of the instantaneous output voltage at said output terminal;

a capacitance element connected between said feedback node and said converter's local ground; and

a comparator which receives V_{fb} at its first input and a voltage V2 which varies with a fixed reference voltage V_{ref} at its second input, said switching control circuit arranged such that at least one of each switching cycle's "on" and "off" time intervals is terminated when V_{fb} crosses V2 due to the natural discharge of the capacitance element through the resistive network, such a time interval being a "modulated" interval; and

a switched noise filter circuit arranged to

apply an offset voltage to said feedback voltage during at least one of each switching cycle's "on" and "off" time intervals and to disconnect said offset voltage from said feedback voltage by the beginning of the immediate modulated interval or shortly thereafter, thereby allowing V_{fb} to decay toward V2, such that the noise margin between V2 and V_{fb} is increased and the effect of extraneous electromagnetic noise coupled into said feedback voltage is reduced.

2. The DC-DC converter of claim 1, wherein said at least one switching element is a transistor connected to provide a conductive path between said input voltage and said first node when on, said converter further comprising a diode connected between said first node and said local ground which conducts the current in said inductor when said switching element is off.

3. The DC-DC converter of claim 1, wherein said at least one switching element comprises a first transistor connected to provide a conductive path between said input voltage and said ,first node when on, and a second transistor connected to provide a conductive path between said first node and said local ground when on, said switching control circuit and said first and second transistors arranged such that said first transistor is on and said second transistor is off during an "on" time interval, and said second transistor is on and said first transistor is off during an "off" time interval, such that said first and second transistors provide synchronous rectification.

4. The DC-DC converter of claim 1, wherein said resistive network is a resistive divider comprising a first resistor connected between said output terminal and said

feedback node, and a second resistor connected between said feedback node and said local ground.

5. The DC-DC converter of claim 1, wherein said capacitance element comprises a capacitor connected between said feedback node and said local ground.

6. The DC-DC converter of claim 1, wherein said switching control circuit further comprises a first monostable multivibrator (MMV) which produces an output arranged to turn on said switching element for a predetermined time interval when the output of said comparator indicates that said feedback voltage has fallen below V2, said predetermined time interval being a switching cycle's "on" time interval T_{on} and the period between the end of said predetermined time interval and the start of the next predetermined time interval being said switching cycle's "off" time interval T_{off} and its modulated interval, such that said converter provides constant-on-time valley-voltage control.

7. The DC-DC converter of claim 6, wherein said switched noise filter circuit comprises:

a voltage source which produces said offset voltage at an output; and

an offset voltage switch which, when closed, connects said offset voltage to said feedback node such that said offset voltage is added to said feedback voltage, said switched noise filter circuit arranged to operate said offset voltage switch such that it is closed during at least a portion of said switching cycle's "on" time interval and is open during said switching cycle's "off" time interval.

8. The DC-DC converter of claim 7, wherein said

switched noise filter circuit is arranged to operate said offset voltage switch such that it is closed for the duration of said switching cycle's "on" time interval.

9. The DC-DC converter of claim 6, wherein said switched noise filter circuit comprises:

a current source which produces a charging current at an output when activated;

said switched noise filter circuit arranged to activate said current source such that said charging current charges said capacitance element during at least a portion of said switching cycle's "on" time interval and to de-activate said current source during said switching cycle's "off" time interval.

10. The DC-DC converter of claim 9, wherein said switched noise filter circuit is arranged to operate said current source such that it is activated for the duration of said switching cycle's "on" time interval.

11. The DC-DC converter of claim 6, wherein said switched noise filter circuit comprises:

a voltage source which produces said offset voltage at an output; and

an offset voltage switch which, when closed, connects said offset voltage to said feedback node such that said offset voltage is added to said feedback voltage, said switched noise filter circuit arranged to operate said offset voltage switch such that it is closed during at least a portion of said "off" time interval and is open during said switching cycle's "on" time interval.

12. The DC-DC converter of claim 11, wherein said switched noise filter circuit is arranged to operate said offset voltage switch at the beginning of said switching

cycle's "off" time interval, such that said offset voltage switch is closed for a time T, with T given by: $T << T_{off}$.

13. The DC-DC converter of claim 11, wherein said switched noise filter circuit further comprises a second MMV which produces an output arranged to close said offset voltage switch for a fixed time interval at the start of said switching cycle's "off" time interval T_{off}.

14. The DC-DC converter of claim 6, wherein said switched noise filter circuit comprises:

a current source which produces a charging current at an output when activated;

said switched noise filter circuit arranged to activate said current source such that said charging current charges said capacitance element during at least a portion of said switching cycle's "off" time interval and to de-activate said current source during said switching cycle's "on" time interval.

15. The DC-DC converter of claim 1, wherein said switching control circuit further comprises a first monostable multivibrator (MMV) which produces an output arranged to turn off said switching element for a predetermined time interval when the output of said comparator indicates that said feedback voltage has risen above V2, said predetermined time interval being a switching cycle's "off" time interval T_{off} and the period between the end of said predetermined time interval and the start of the next predetermined time interval being said switching cycle's "on" time interval T_{on} and its modulated interval, such that said converter provides constant-off-time peak-voltage control.

16. The DC-DC converter of claim 15, wherein said switched noise filter circuit comprises:

a voltage source which produces said offset voltage at an output; and

an offset voltage switch which, when closed, connects said offset voltage to said feedback node such that said offset voltage is subtracted from said feedback voltage, said switched noise filter circuit arranged to operate said offset voltage switch such that it is closed during at least a portion of said switching cycle's "off" time interval and is open during said switching cycle's "on" time interval.

17. The DC-DC converter of claim 16, wherein said switched noise filter circuit is arranged to operate said switching element such that it is closed for the duration of said switching cycle's "off" time interval.

18. The DC-DC converter of claim 15, wherein said switched noise filter circuit comprises:

a current source which produces a discharging current at an output when activated;

said switched noise filter circuit arranged to activate said current source such that said discharging current discharges said capacitance element during at least a portion of said switching cycle's "off" time interval and to de-activate said current source during said switching cycle's "on" time interval.

19. The DC-DC converter of claim 15, wherein said switched noise filter circuit comprises:

a voltage source which produces said offset voltage at an output; and

an offset voltage switch which, when closed, connects said offset voltage to said feedback node such

that said offset voltage is subtracted from said feedback voltage, said switched noise filter circuit arranged to operate said offset voltage switch such that it is closed during at least a portion of said "on" time interval and is open during said switching cycle's "off" time interval.

20. The DC-DC converter of claim 19, wherein said switched noise filter circuit is arranged to operate said offset voltage switch at the beginning of said switching cycle's "on" time interval, such that said offset voltage switch is closed for a time T, with T given by: $T << T_{on}$.

21. The DC-DC converter of claim 19, wherein said switched noise filter circuit further comprises a second MMV which produces an output arranged to close said offset voltage switch for a fixed time interval at the start of said switching cycle's "on" time interval T_{on}.

22. The DC-DC converter of claim 1, wherein said switching control circuit further comprises a set-reset latch which is connected to the output of said comparator at its set input and to a periodic clock signal at its reset input, said latch arranged to be set and turn on said switching element when the output of said comparator indicates that said feedback voltage has fallen below V_{ref} and to be reset and turn off said switching element in response to said periodic clock signal, the time said switching element is turned on being a switching cycle's "on" time interval T_{on} and the period between the end of said "on" time interval and the start of the next "on" time interval being said switching cycle's "off" time interval T_{off} and its modulated interval, such that said converter provides constant-frequency valley-voltage control.

23. The DC-DC converter of claim 22, wherein said switched noise filter circuit comprises:

a voltage source which produces said offset voltage at an output; and

an offset voltage switch which, when closed, connects said offset voltage to said feedback node such that said offset voltage is added to said feedback voltage, said switched noise filter circuit arranged to operate said offset voltage switch such that it is closed during at least a portion of said switching cycle's "on" time interval and is open during said switching cycle's "off" time interval.

24. The DC-DC converter of claim 22, wherein said switched noise filter circuit comprises:

a current source which produces a charging current at an output when activated;

said switched noise filter circuit arranged to activate said current source such that said charging current charges said capacitance element during at least a portion of said switching cycle's "on" time interval and to de-activate said current source during said switching cycle's "off" time interval.

25. The DC-DC converter of claim 22, wherein said switched noise filter circuit comprises:

a voltage source which produces said offset voltage at an output; and

an offset voltage switch which, when closed, connects said offset voltage to said feedback node such that said offset voltage is added to said feedback voltage, said switched noise filter circuit arranged to operate said offset voltage switch such that it is closed during at least a portion of said "off" time interval and is open during said switching cycle's "on" time interval.

26. The DC-DC converter of claim 25, wherein said switched noise filter circuit is arranged to operate said offset voltage switch at the beginning of said switching cycle's "off" time interval, such that said offset voltage switch is closed for a time T, with T given by:
$T << T_{off}$.

27. The DC-DC converter of claim 1, wherein said comparator has an associated hysteresis voltage V_{hyst}, the output of said comparator arranged to turn on said switching element when the output of said comparator indicates that said feedback voltage has fallen below $V_{ref} - (V_{hyst}/2)$, and to turn off said switching element when the output of said comparator indicates that said feedback voltage has risen above said $V_{ref} + (V_{hyst}/2)$, the time said switching element is turned on being a switching cycle's "on" time interval T_{on} and a modulated interval and the time said switching element is turned off being said switching cycle's "off" time interval T_{off} and a modulated interval, such that said converter provides hysteretic control.

28. The DC-DC converter of claim 27, wherein said switched noise filter circuit comprises:

a first voltage source which produces a first offset voltage at an output;

a first offset voltage switch which, when closed, connects said first offset voltage to said feedback node such that said first offset voltage is subtracted from said feedback voltage,

a second voltage source which produces a second offset voltage at an output; and

a second offset voltage switch which, when closed, connects said second offset voltage to said

feedback node such that said second offset voltage is added to said feedback voltage;

said switched noise filter circuit arranged to operate said first offset voltage switch such that it is closed during at least a portion of said switching cycle's "on" time interval and is open during said switching cycle's "off" time interval, and to operate said second offset voltage switch such that it is closed during at least a portion of said switching cycle's "off" time interval and is open during said switching cycle's "on" time interval.

29. The DC-DC converter of claim 28, wherein said switched noise filter circuit is arranged to operate said first offset voltage switch at the beginning of said switching cycle's "on" time interval such that said first offset voltage switch is closed for a time T1, with T1 given by:

$T1 << T_{on}$,

and to operate said second offset voltage switch at the beginning of said switching cycle's "off" time interval such that said second offset voltage switch is closed for a time T2, with T2 given by:

$T2 << T_{on}$.

30. The DC-DC converter of claim 1, further comprising a voltage error amplifier which produces an error voltage that varies with the difference between a voltage representative of the instantaneous output voltage and V_{ref}, said error voltage being said voltage V2;

wherein said switching control circuit further comprises a first monostable multivibrator (MMV) which produces an output arranged to turn off said switching element for a predetermined time interval when the output of said comparator indicates that said feedback voltage has

risen above V2, said predetermined time interval being a switching cycle's "off" time interval T_{off} and the period between the end of said predetermined time interval and the start of the next predetermined time interval being said switching cycle's "on" time interval T_{on} and its modulated interval, such that said converter provides constant-off-time Vsquare control.

31. The DC-DC converter of claim 30, wherein said switched noise filter circuit comprises:

a voltage source which produces said offset voltage at an output; and

an offset voltage switch which, when closed, connects said offset voltage to said feedback node such that said offset voltage is subtracted from said feedback voltage, said switched noise filter circuit arranged to operate said offset voltage switch such that it is closed during at least a portion of said switching cycle's "off" time interval and is open during said switching cycle's "on" time interval.

32. The DC-DC converter of claim 30, wherein said switched noise filter circuit comprises:

a current source which produces a discharging current at an output when activated;

said switched noise filter circuit arranged to activate said current source such that said discharging current discharges said capacitance element during at least a portion of said switching cycle's "off" time interval and to de-activate said current source during said switching cycle's "on" time interval.

33. The DC-DC converter of claim 30, wherein said switched noise filter circuit comprises:

a voltage source which produces said offset

voltage at an output; and

an offset voltage switch which, when closed, connects said offset voltage to said feedback node such that said offset voltage is subtracted from said feedback voltage, said switched noise filter circuit arranged to operate said offset voltage switch such that it is closed during at least a portion of said "on" time interval and is open during said switching cycle's "off" time interval.

34. The DC-DC converter of claim 33, wherein said switched noise filter circuit is arranged to operate said offset voltage switch at the beginning of said switching cycle's "on" time interval, such that said offset voltage switch is closed for a time T, with T given by:

$T << T_{on}$.